CLAIMS

What is claimed is:

1. A central processing unit (CPU) comprising:

a translation looksaside buffering; and

a mapping logic function to predict a set index value for the TLB prior to the generation of an effective address.

2. The CPU of claim 1 wherein the mapping logic function distributes entries within the TLB throughout the TLB.

3. The CPU of claim 1 wherein the mapping logic comprises a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual address, where N is smaller than the number of bits in a virtual address.

4. The CPU of claim 1 wherein the mapping logic comprises an Exclusive-or of some number of base-register bits and some number of offset bits of a virtual address.

5. The CPU of claim 1 further comprising a register interface having one or more registers to control the TLB.

6. The CPU of claim 5 wherein the one or more registers within the register interface chooses an entry within the TLB to be accessed.

7. The CPU of claim 1 wherein the predicted set index may differ from the effective address without requiring recovery actions if the predicted set index and the effective address differ.

8. The CPU of claim 1 wherein mapping logic function includes a first set of bits from instruction and a second set of bits from base and offset addresses.

9. The CPU of claim 1 wherein the effective address being mapped is the address of an instruction that is being fetched for execution.

10. The CPU of claim 1 wherein the effective address being mapped is the address of data being read or written by the processor.

11. The CPU of claim 1 wherein the mapping logic function includes control signals received from the processor and bits received from the generation of the effective address.

12. The CPU of claim 11 wherein the mapping logic combines the signals and the bits using a hash to predict a set to look up the translation for the predicted address.

13. A method comprising:

looking up a register at a register interface; and

predicting a set index value for a translation lookaside buffer (TLB) at a

mapping logic function prior to the generation of an effective address.

14. The method of claim 13 further comprising performing a lookup of the TLB using the predicted set index.

15. The method of claim 13 further comprising calculating an effective address.

16. The method of claim 13 wherein the predicted set index differs from the effective address.

17. A computer system comprising central processing unit (CPU) having a mapping logic function to predict a set index value for a translation lookaside buffer (TLB) prior to the generation of an effective address.

18. The computer system of claim 17 wherein the mapping logic function distributes entries within the TLB throughout the TLB.

19. The computer system of claim 17 wherein the mapping logic function comprises a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual address, where N is smaller than the number of bits in a virtual address.

20. The computer system of claim 17 wherein the mapping logic function comprises an Exclusive-or of some number of base-register bits and some number of offset bits of a virtual address.

21. The computer system of claim 17 further comprising a register interface having one or more registers to control the TLB.

22. The computer system of claim 21 wherein the one or more registers within the register interface chooses an entry within the TLB to be accessed.

23. The computer system of claim 17 wherein the mapping logic function includes control signals received from the processor and bits received from the generation of the effective address.

24. The computer system of claim 23 wherein the mapping logic combines the signals and the bits using a hash to predict a set to look up the translation for the predicted address.

25. A computer system comprising:

central processing unit (CPU) having a mapping logic function to predict a set index value for a translation lookaside buffer (TLB) prior to the generation of an effective address;

a chipset coupled to the CPU and

a main memory coupled to the chipset.

26. The computer system of claim 25 wherein the mapping logic function distributes entries within the TLB throughout the TLB.

27. The computer system of claim 25 wherein the mapping logic comprises a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual address, where N is smaller than the number of bits in a virtual address.